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Docker No.: 063979-0035

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

Kenji TOYODA, et al. : Confirmation Number: 4380

Application No.: 10/684,419 : Group Art Unit: 2818
Patent No.: 6,847,543

Filed: October 15, 2003 : Examiner: H. Hoang
Issued: January 25, 2005

For: A NON-VOLATILE MEMORY CIRCUIT, A METHOD FOR DRIVING THE SAME, AND A SEMICONDUCTOR DEVICE USING THE MEMORY CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop Box 4 / Certificate of Correction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
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of Correction

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, Claims 5 and 7 (formerly numbered 17 and 19) have typographical errors as indicated on attached Form 1050. The correct versions of the respective text can be seen on the attached copies of Applicant's Preliminary Amendment dated February 12, 2004 as well as on Page 59 of the originally filed claims, showing claim 19, now renumbered Claim 7.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
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Date: May 24, 2005

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PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,543 B2

DATED : January 25, 2005

INVENTOR(S) : Kenji TOYODA, et al.

It is certified that error appears in the above-identified patent and that said Letter Patent is hereby corrected as shown below:

IN THE CLAIMS

Claim 5, Column 18, line 65, change "according to claim 1, which " to -- according to claim 1, in which --;

Claim 7, Column 20, lines 1 & 2, change
"the circuit further comprising a third resistor element and a fourth resistor element; said third resistor element" to
-- the circuit further comprising a third resistor element and a fourth resistor element;
said third resistor element --;

Claim 7, Column 20, line 9, change "whose resistance value can be: changed by heat" to -- whose resistance value can be changed by heat --.

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said first and second resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising a third step wherein a ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

the second step comprising a fourth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of said word line is changed from a high level to a low level, and then the voltage of said word line is changed from a high level to a low level after a second period.

19. A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is said first positional relationship;

the circuit further comprising a third resistor element and a fourth resistor element;

said third resistor element being connected between the source of said second transistor and said power line, and said fourth resistor element being connected between the source of said fourth transistor and said power line;

said first to fourth resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising:

a third step wherein a supply voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

a fourth step wherein the ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a second period;

the second step comprising:

a fifth step wherein the supply voltage is applied to said second bit line, a voltage lower than the supply voltage is applied to said first bit line, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a third period; and

a sixth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of the word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a fourth period.

20. A semiconductor device using the non-volatile memory circuit of claim 1 as a memory for storing parameters of a look-up table.

21. A semiconductor device using the non-volatile memory circuit of claim 1 as a memory for controlling circuit interconnection information.

22. A semiconductor device for encryption comprising the non-volatile memory circuit of claim 1.

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Docket No.: 63979-035

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Kenji TOYODA, et al.	:	Confirmation Number: 4380
Serial No.: 10/684,419	:	Group Art Unit: 2818
Filed: October 15, 2003	:	Examiner:

For: A NON-VOLATILE MEMORY CIRCUIT, A METHOD FOR DRIVING THE SAME, AND A SEMICONDUCTOR DEVICE USING THE MEMORY CIRCUIT

PRELIMINARY AMENDMENT

Mail Stop Preliminary Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to the examination of the above-identified application, please amend the application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

1-12. (Cancelled)

13. (Original) A method for driving a non-volatile memory circuit comprising:

a first inverter which comprises a first transistor and a second transistor each having a gate and a drain, the gates of said first and second transistors being connected to each other, and the drains of said first and second transistors being connected to each other with a first node therebetween;

a second inverter which comprises a third transistor and a fourth transistor each having a gate and a drain, the gates of said third and fourth transistors being connected to each other, and the drains of said third and fourth transistors being connected to each other with a second node therebetween;

a fifth transistor which comprises a gate and is connected between a first bit line and said first node, said gate being connected to a word line; and

a sixth transistor which comprises a gate and is connected between a second bit line and said second node, said gate being connected to said word line;

said first node being connected to the gate of said third transistor and to the gate of said fourth transistor;

said second node being connected to the gate of said first transistor and to the gate of said second transistor;

the source of said first transistor and the source of said third transistor being connected to a ground line;

the source of said second transistor and the source of said fourth transistor being connected to a power line;

the circuit further being provided with a first resistor element and a second resistor element whose resistance values can be electrically modified;

the positional relationship of said first resistor element and said second resistor element being selected from the following first to fourth positional relationships:

a first positional relationship in which said first resistor element is connected between the source of said first transistor and said ground line, and said second resistor element is connected between the source of said third transistor and said ground line;

a second positional relationship in which said first resistor element is connected between the source of said second transistor and said power line, and said second resistor element is connected between the source of said fourth transistor and said power line;

a third positional relationship in which said first resistor element is connected between said first node and the drain of said first transistor, and said second resistor element is connected between said second node and the drain of said third transistor; and

a fourth positional relationship in which said first resistor element is connected between said first node and the drain of said second transistor, and said second resistor element is connected between said second node and the drain of said fourth transistor;

the method comprising:

a STORE step including a first step wherein the resistance values of said first and second resistor elements are reduced to low levels before power to said non-volatile memory circuit is removed; and a second step, which follows said first step, wherein the resistance value of one of said first and second resistor elements is increased to a high level; and

a RECALL step wherein voltages are applied to said word line, said first and second bit lines and said power line at a predetermined time after power supply to said non-volatile memory circuit is started.

14. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein said word line is set at a high voltage level, and the voltages applied to said power line, said first bit line and said second bit line are slowly increased to the supply voltage level.

15. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein predetermined voltages are applied to said first and second bit lines, and, in this state, said word line is set to a high voltage level, and the voltage applied to said power line is slowly increased to the supply voltage level.

16. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein predetermined voltages are applied to said first and second bit lines, and, in this state, the voltage applied to the word line is slowly increased to a high level, and the voltage applied to said power line is slowly increased to the supply voltage level.

new claim ⑤

17. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is either of said first positional relationship or said third

positional relationship;

said first and second resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step further comprising a third step wherein a supply voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and the voltage of said word line is changed from a high level to a low level after a first period; and

the second step further comprising a fourth step wherein the supply voltage is applied to said first bit line, a voltage lower than the supply voltage is applied to said second bit line, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a second period.

18. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is either said second positional relationship or said fourth positional relationship;

said first and second resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising a third step wherein a ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

the second step comprising a fourth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of said word line is changed from a high level to a low level, and then the voltage of said word line is changed from a high level to a low level after a second period.

new claim ⑦

19. (Original) A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is said first positional relationship;

the circuit further comprising a third resistor element and a fourth resistor element; said third resistor element being connected between the source of said second transistor and said power line, and said fourth resistor element being connected between the source of said fourth transistor and said power line;

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said first to fourth resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising:

a third step wherein a supply voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

a fourth step wherein the ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a second period;

the second step comprising:

a fifth step wherein the supply voltage is applied to said second bit line, a voltage lower than the supply voltage is applied to said first bit line, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a third period; and

a sixth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of the word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a fourth period.

20-22. (Cancelled)

REMARKS

In the foregoing preliminary amendment, claims 1-12 and 20-22 have been cancelled, without prejudice. No new matter has been added. Entry of the foregoing amendment is respectfully requested.

Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: February 12, 2004

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